Figure 4 is perfect, the voltage that has been read during the period C must correctly correspond to the signal charge amount. In actual, however, during the period D after the resetting, the output voltage of the CSA 20 is not perfectly equal to the reference voltage GND, thereby causing the generation of an offset voltage. Such an offset voltage is generated due to (a) an offset or a flicker noise of the operational amplifier 20a and/or (b) a feed through phenomenon occurred when the TFT (switching devices 18) and/or the reset switch 20c turn on and off. The field through phenomenon is essential to MOS switches. According to

**IN THE CLAIMS:**

Please cancel Claims 3 and 5.

Please amend Claims 1, 4, 6, 7, 10, and 11 as follows:

1. (Amended) A charge amount detection circuit, comprising:

a charge sensitive amplifier;

a low pass filter circuit provided so as to follow the charge sensitive amplifier; and

a voltage amplifier circuit provided so as to follow the low pass filter circuit,

wherein one part of circuit elements constituting the low pass filter circuit and one part of circuit elements constituting the voltage amplifier circuit are commonly used;

wherein the low pass filter circuit and the voltage amplifier circuit share a plurality of capacitors that are connected with each other in parallel; and

a switch for switching between a state in which at least one of the capacitors are inserted in the charge amount detection circuit and a state in which said at least one of the capacitors are not inserted.

4. (Amended) The charge amount detection circuit as set forth in claim 1,

wherein the voltage amplifier circuit includes an operational amplifier having an inverted input terminal to which the capacitor is connected, and

the low pass filter circuit includes a resistor and the plurality of capacitors are connected in series with the resistor.

6. (Amended) The charge amount detection circuit as set forth in claim 1,

wherein an amplification of the voltage amplifier circuit is 1 when the state in which said at least one of the capacitors are not inserted is made by the switch.

7. (Amended) The charge amount detection circuit as set forth in claim 1,

wherein a plurality of switches for respective switching between a state in which at least one of the capacitors are inserted in the charge amount detection circuit and a state in which said at least one of the capacitors are not inserted, numbers of the capacitors that are switched by the respective switches being different from each other.

10. (Amended) The charge amount detection circuit as set forth in claim 1, further comprising:

a sampling hold circuit for holding a signal charge outputted from the voltage amplifier circuit;

an analog to digital converter for analog to digital converting the signal charge that has held by the sampling hold circuit;

a multiplexer for assigning a plurality of input terminals to the analog to digital converter; and

a data latch circuit for holding the signal charge that has been converted into a digital value.

11. (Amended) A two-dimensional image sensor having a charge amount detection circuit, said circuit comprising:

a charge sensitive amplifier;

a low pass filter circuit provided so as to follow the charge sensitive amplifier; and

a voltage amplifier circuit provided so as to follow the low pass filter circuit,

wherein one part of circuit elements constituting the low pass filter circuit and one part of circuit elements constituting the voltage amplifier circuit are commonly used;

wherein the low pass filter circuit and the voltage amplifier circuit share a plurality of capacitors that are connected with each other in parallel; and

a switch for switching between a state in which at least one of the capacitors are inserted in the charge amount detection circuit and a state in which said at least one of the capacitors are not inserted.